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10/731,018	12/10/2003	Takayuki Iwasa	25873	5199

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EXAMINER	
NGUYEN, HOAN C	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 10/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/731,018	IWASA, TAKAYUKI	
	Examiner	Art Unit	
	HOAN C. NGUYEN	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *01 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) *4 and 5* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01/13/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of Species I in the reply filed on 01 September 2005 is acknowledged.

Claims 4-5 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected Species, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 01 September 2005.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-3 are rejected under 35 U.S.C. 102(b) as being anticipated by Hideo et al. (JP09-171195) provided by applicants' IDS.

In regard to claim 1, Hideo et al. disclose (Figs. 10-17, 18 and 21) a reflective liquid crystal display having

- a semiconductor substrate 1,
- a plurality of switching elements 2 formed on the semiconductor substrate and electrically isolated from one another,
- a plurality of functional films 4a/4b formed one upon another over the switching elements,

- a plurality of reflective pixel electrodes 8a formed on a top one of the functional films and electrically isolated from one another to correspond to the switching elements, respectively,
- storage capacitors 3 provided for the switching elements,
- each switching element 2, each reflective pixel electrode 8 connected to the switching element, and
- each storage capacitor 3 for the switching element constituting a pixel, pixels being arranged in a matrix on the semiconductor substrate,
- a transparent substrate (glass substrate 22),
- a transparent counter electrode 23 formed on a reverse of the transparent substrate to face the reflective pixel electrodes, and
- liquid crystals 30 inherently sealed between the reflective pixel electrodes and the counter electrode,

the reflective liquid crystal display comprising:

- at least two layers of light blocking metal films 52/53 that are formed one upon another between the semiconductor substrate 1 and the reflective pixel electrodes 8a with an insulating film 4a being laid on and under each layer of the light blocking metal films, to block part of read light 42, which has been made incident from the transparent substrate side to the liquid crystals through the counter electrode and has penetrated the insulating film adjacent to the reflective pixel electrodes through openings formed between adjacent ones of the reflective pixel electrodes, from reaching the switching elements,

- any one layer of the light blocking metal films 52 covering the openings formed between adjacent ones of the reflective pixel electrodes, the light blocking metal films in each layer being electrically isolated from one another pixel by pixel,
- each light blocking metal film in each layer being electrically connected, through via holes, to each corresponding one of the switching elements, reflective pixel electrodes, and storage capacitors.

wherein

Claim 2:

- a storage capacitance value of the storage capacitor in each pixel is the sum of a storage capacitance value of a storage capacitor consisting of a diffused capacitor electrode 8a, an insulating film 4a/4b, a capacitor electrode 9a, and a capacitor electrode contact 10 formed on the semiconductor substrate and a storage capacitance value of a storage capacitor consisting of the two layers of the light blocking metal films and the light blocking insulating film formed between the two layers of the light blocking metal films.

Claim 3:

- at least one of the two layers of the light blocking metal films 52/53 is made of a material selected from the group consisting of TiN, Ti, and layered TiN/Ti.

2. Claims 1-3 are rejected under 35 U.S.C. 102(b) as being anticipated by Takayuki (JP2000-193994) provided by applicants' IDS.

In regard to claim 1, Takayuki discloses (Fig. 1) a reflective liquid crystal display having

- a semiconductor substrate 1,
- a plurality of switching elements 2 formed on the semiconductor substrate and electrically isolated from one another,
- a plurality of functional films 4 formed one upon another over the switching elements,
- a plurality of reflective pixel electrodes 15 formed on a top one of the functional films and electrically isolated from one another to correspond to the switching elements, respectively,
- storage capacitors 3 provided for the switching elements,
- each switching element 2, each reflective pixel electrode 15 connected to the switching element, and
- each storage capacitor 3 for the switching element constituting a pixel, pixels being arranged in a matrix on the semiconductor substrate,
- a transparent substrate (glass substrate 17),
- a transparent counter electrode formed on a reverse of the transparent substrate to face the reflective pixel electrodes, and
- liquid crystals 16 inherently sealed between the reflective pixel electrodes and the counter electrode,

the reflective liquid crystal display comprising:

- at least two layers of light blocking metal films 13/14 that are formed one upon another between the semiconductor substrate 1 and the reflective pixel electrodes 15 with an insulating film 4 being laid on and under each layer of the

light blocking metal films, to block part of read light, which has been made incident from the transparent substrate side to the liquid crystals through the counter electrode and has penetrated the insulating film adjacent to the reflective pixel electrodes through openings 15a formed between adjacent ones of the reflective pixel electrodes, from reaching the switching elements,

- any one layer of the light blocking metal films 13/14 covering the openings 15a formed between adjacent ones of the reflective pixel electrodes, the light blocking metal films in each layer being electrically isolated from one another pixel by pixel,
- each light blocking metal film in each layer being electrically connected, through via holes, to each corresponding one of the switching elements, reflective pixel electrodes, and storage capacitors.

wherein

Claim 2:

- a storage capacitance value of the storage capacitor in each pixel is the sum of a storage capacitance value of a storage capacitor consisting of a diffused capacitor electrode 15, an insulating film 4, a capacitor electrode 11, and a capacitor electrode contact formed on the semiconductor substrate and a storage capacitance value of a storage capacitor consisting of the two layers of the light blocking metal films and the light blocking insulating film formed between the two layers of the light blocking metal films.

Claim 3:

- at least one of the two layers of the light blocking metal films 14 is made of a material selected from the group consisting of TiN, Ti, and layered TiN/Ti.

3. Claims 1-2 are rejected under 35 U.S.C. 102(b) as being anticipated by Katsumi et al. (JP2002-040482) provided by applicants' IDS.

In regard to claim 1, Katsumi et al. disclose (Fig. 1) a reflective liquid crystal display having

- a semiconductor substrate 31,
- a plurality of switching elements formed on the semiconductor substrate and electrically isolated from one another,
- a plurality of functional films 41-47 formed one upon another over the switching elements,
- a plurality of reflective pixel electrodes 5 formed on a top one of the functional films and electrically isolated from one another to correspond to the switching elements, respectively,
- storage capacitors provided for the switching elements,
- each switching element, each reflective pixel electrode 15 connected to the switching element, and
- each storage capacitor for the switching element constituting a pixel, pixels being arranged in a matrix on the semiconductor substrate,
- a transparent substrate 2,

- a transparent counter electrode formed on a reverse of the transparent substrate to face the reflective pixel electrodes, and
- liquid crystals 3 inherently sealed between the reflective pixel electrodes and the counter electrode,

the reflective liquid crystal display comprising:

- at least two layers of light blocking metal films 44/46 that are formed one upon another between the semiconductor substrate 31 and the reflective pixel electrodes 5 with an insulating film 43/45/47 being laid on and under each layer of the light blocking metal films, to block part of read light, which has been made incident from the transparent substrate side to the liquid crystals through the counter electrode and has penetrated the insulating film adjacent to the reflective pixel electrodes through openings formed between adjacent ones of the reflective pixel electrodes, from reaching the switching elements,
- any one layer of the light blocking metal films 44/46 covering the openings 15a formed between adjacent ones of the reflective pixel electrodes, the light blocking metal films in each layer being electrically isolated from one another pixel by pixel,
- each light blocking metal film in each layer being electrically connected, through via holes, to each corresponding one of the switching elements, reflective pixel electrodes, and storage capacitors.

wherein

Claim 2:

- a storage capacitance value of the storage capacitor in each pixel is the sum of a storage capacitance value of a storage capacitor consisting of a diffused capacitor electrode, an insulating film 41/43/45/47, a capacitor electrode, and a capacitor electrode contact formed on the semiconductor substrate and a storage capacitance value of a storage capacitor consisting of the two layers of the light blocking metal films and the light blocking insulating film formed between the two layers of the light blocking metal films.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-3 are rejected under 35 U.S.C. 102(e) as being anticipated by Fumitoshi et al. (JP2002-357820) provided by applicants' IDS.

In regard to claim 1, Fumitoshi et al. disclose (Fig. 10) a reflective liquid crystal display having

- a semiconductor substrate 1,
- a plurality of switching elements formed on the semiconductor substrate and electrically isolated from one another,
- a plurality of functional films 18/25/71/73/41/35/39 formed one upon another over the switching elements,

- a plurality of reflective pixel electrodes 41 formed on a top one of the functional films and electrically isolated from one another to correspond to the switching elements, respectively,
- storage capacitors provided for the switching elements,
- each switching element, each reflective pixel electrode 41 connected to the switching element, and
- each storage capacitor for the switching element constituting a pixel, pixels being arranged in a matrix on the semiconductor substrate,
- a transparent substrate (glass substrate 61),
- a transparent counter electrode 55 formed on a reverse of the transparent substrate to face the reflective pixel electrodes, and
- liquid crystals 51 inherently sealed between the reflective pixel electrodes and the counter electrode,

the reflective liquid crystal display comprising:

- at least two layers of light blocking metal films 37/38 that are formed one upon another between the semiconductor substrate 1 and the reflective pixel electrodes 15 with an insulating film 35/39 being laid on and under each layer of the light blocking metal films, to block part of read light, which has been made incident from the transparent substrate side to the liquid crystals through the counter electrode and has penetrated the insulating film adjacent to the reflective pixel electrodes through openings (between RE 41) formed between adjacent ones of the reflective pixel electrodes, from reaching the switching elements,

- any one layer of the light blocking metal films 37/38 covering the openings 15a formed between adjacent ones of the reflective pixel electrodes, the light blocking metal films in each layer being electrically isolated from one another pixel by pixel,
- each light blocking metal film in each layer being electrically connected, through via holes, to each corresponding one of the switching elements, reflective pixel electrodes, and storage capacitors.

wherein

Claim 2:

- a storage capacitance value of the storage capacitor in each pixel is the sum of a storage capacitance value of a storage capacitor consisting of a diffused capacitor electrode, an insulating film, a capacitor electrode, and a capacitor electrode contact formed on the semiconductor substrate and a storage capacitance value of a storage capacitor consisting of the two layers of the light blocking metal films and the light blocking insulating film formed between the two layers of the light blocking metal films.

Claim 3:

- at least one of the two layers of the light blocking metal films 37/38 is made of a material selected from the group consisting of TiN, Ti, and layered TiN/Ti.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Libsch et al. (US 6181398 B1) disclose a LCD reflection display array implementing two or more layers of reflecting front surface mirrors with an upper layer mirror(s) having bsorbing back surface(s). The mirror surfaces associated with each pixel are electrically connected to the pixel output electrode. The lower mirrors are appropriately positioned in the three dimensions to achieve nearly 100% aperture fill.

Cacharelis (US 6437839 B1) discloses a liquid crystal on silicon (LCOS) display pixel with dual storage capacitors for increasing the storage capacitance of the charge storage node for the liquid crystal pixel. The two capacitors are in a stacked arrangement. The bottom capacitor is formed by using a buried diffusion layer as the bottom electrode, a first layer of polysilicon (poly) as the top electrode and silicon dioxide as the dielectric. The top capacitor is a poly-to-poly capacitor formed by using the first layer of poly as the bottom electrode and a second layer of poly as the top electrode.

Sato et al. (US 6693691 B2) disclose a liquid crystal light valve includes a semiconductor substrate having a region for a plurality of switching elements formed in a matrix form. A first metal layer is formed on the surface of the semiconductor substrate through an insulating layer and divided into a plurality of parts by first slits. A second metal layer is formed on the first metal layer through another insulating layer and divided into a plurality of parts by second slits. A third metal layer is formed on the

second metal layer through still another insulating layer and divided into a plurality of parts by third slits. An opposite substrate has an opposite electrode on a surface thereof, disposed so as to be opposite to said third metal layer through an interval on the opposite electrode side. Liquid crystal fills the interval between said opposite electrode and the third metal layer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HOAN C. NGUYEN whose telephone number is (571) 272-2296. The examiner can normally be reached on MONDAY-THURSDAY:8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim H. Robert can be reached on (571) 272-2293. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HOAN C. NGUYEN
Examiner
Art Unit 2871

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ANDREW SCHECHTER
PRIMARY EXAMINER